Cancelled Claims

Claims 1, 4-6, 20-23, 29-40, 49, and 53-64 will be cancelled upon entry of the present amendment. The applicant has cancelled these claims to reduce the number of issues outstanding in this application to more quickly obtain a notice of allowance. However, the applicant respectfully submits that the cancelled claims 1, 4-6, 20-23, 29-40, 49, and 53-64 are not disclosed or suggested by the prior art, and are in condition for allowance.

Double Patenting

The Examiner provisionally rejected claims 1-6 under the judicially created doctrine of obviousness-type double patenting over claims 11-18 of copending Application Serial No. 08/902,843. Claims 1 and 4-6 will be cancelled upon entry of the present amendment. The applicant respectfully submits that claims 2 and 3 are patentably distinct from the claims in Application Serial No. 08/902,843. The applicant respectfully requests that this provisional rejection be withdrawn.

Rejection of Claims under 35 USC §102

Claim 68 was rejected under 35 USC § 102(a) as being anticipated by Sugita (JP Patent No. 08-255878). The applicant respectfully traverses.

Claim 68 recites a transistor comprising, among other elements, a channel region in a substrate, a floating gate, and means for separating the floating gate from the channel region.

Claim 68 is a means-plus-function claim under 35 U.S.C. § 112, paragraph 6. The PTO has promulgated "Supplemental Examination Guidelines for Determining the Applicability of 35 U.S.C. 112, paragraph 6" at 65 FR 38510. The Guidelines require the Examiner to make a prima facie case of equivalence under paragraph 6. However, the Examiner has not presented an explanation or a rationale as to why the disclosure of Sugita is equivalent to the corresponding elements disclosed in the specification as is required by the Guidelines.

The applicant respectfully submits that Sugita does not disclose an equivalent to the corresponding elements disclosed in the specification under 35 U.S.C. § 112, paragraph 6. Sugita does not anticipate claim 68, and therefore claim 68 is in condition for allowance.

Claims 4, 5, 20, 23, 29, 32 and 36 were rejected under 35 USC § 102(b) as being anticipated by or, in the alternative, as obvious in view of Sakata et al. (Electronics Letters, Vol. 30 No. 9, pp.688-689, Sakata). Claims 4, 5, 20, 23, 29, 32 and 36 have been cancelled.

Rejection of Claims under §103

Claims 1-3, 6, 21, 22, 24-30, 33-34, 37, 39, 41, 44-46, 50 and 65 were rejected under 35 USC § 103(a) as being unpatentable over Sakata. The applicant respectfully traverses.

Claims 1, 6, 21, 22, 29, 30, 33, 34, 37, and 39 have been cancelled.

Claim 24 recites a transistor comprising a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate, and a gate separated from the channel region by a layer of amorphous carburized silicon that was grown on the substrate.

Sakata is deficient as a reference in that Sakata does not disclose a source region in a substrate, a drain region in the substrate, a channel region between the source region and the drain region in the substrate as are recited in claim 24.

The Examiner stated that the claimed structure including the recited source region, drain region, and channel region would have been obvious to one skilled in the art in view of Sakata. The applicant respectfully traverses.

"To establish a *prima facie* case of obviousness ... there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." MPEP 2143. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP 2143.01.

"When a rejection [under section 103] depends on a combination of prior art references, there must be some teaching, suggestion, or motivation to combine the references." *In re Rouffet,* 47 USPQ2d 1453, 1456 (Fed. Cir. 1998). The court elaborated:

> "rejecting patents solely by finding prior art corollaries for the claimed elements would permit an examiner to use the claimed invention itself as a blueprint for piecing together

> elements in the prior art to defeat the patentability of the claimed invention. Such an approach would be "an illogical and inappropriate process by which to determine patentability".....To prevent the use of hindsight based on the invention to defeat patentability of the invention, this court requires the examiner to show a motivation to combine the references that create the case of obviousness. In other words, the examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed....This court forbids the use of hindsight in the selection of references that comprise the case of obviousness." *In re Rouffet,* 47 USPQ2d at 1457-1458.

The "case law makes clear that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references." *Ecolochem Inc. v. Southern California Edison,* 56 USPQ2d 1065, 1073 (Fed. Cir. 2000). There must be a "clear and particular" showing of a "teaching or motivation to combine prior art references." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). "[A] lofty level of skill alone does not suffice to supply a motivation to combine." *In re Rouffet,* 47 USPQ2d at 1459. "Determining whether there is a suggestion or motivation to modify a prior art reference is one aspect of determining the scope and content of the prior art." *Ruiz v. A. B. Chance Co.,* 57 USPQ2d 1161, 1167 (Fed. Cir. 2000).

The Examiner's position is that one skilled in the art would have found it obvious to add to Sakata features from known transistors, specifically a source region, a drain region, and a channel region. The applicant respectfully submits that the Examiner is improperly using hindsight in rejecting claims 2, 3, 24-28, 41, 44-46, 50, and 65 under section 103. The Examiner has not supplied a sufficient suggestion from Sakata, the only applied prior art, to support the allegation that the addition of the recited source region, drain region, and channel region to Sakata would have been obvious to one skilled in the art.

The whole disclosure of Sakata teaches away from the modification proposed by the Examiner. Sakata discloses in Figure 1 a diode structure comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Column 3. Both a-SiC:H and a-Si:H are highly resistive, insulating layers. Both are hydrogenated to ensure high resistivity. A plot of capacitance-voltage (C-V) characteristics for the diode is shown in Fig. 2 of Sakata. The plot

shows that the "capacitance at 3V (470pF) is in fairly good agreement with the calculated capacitance of stacked insulator layers." Sakata, column 2. Sakata is disclosing a diode structure comprised entirely of "stacked insulator layers" that has a capacitance.

Sakata discloses that both electrons and holes "can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces." Sakata, column 1. However, Sakata has not substantially identified the mechanism for the charge storage: "We speculate that traps in the a-Si:H and/or at the interface between a-Si:H and a-SiC:H are acting as memory sites." Sakata, column 2. The band edges shown in Figure 1 are also pure speculation by Sakata: "However, we speculate that a band offset exists at both band edges in the present samples, as schematically shown in Fig. 1, because both electrons and holes are stored in the a-Si:H layer." Sakata, column 2. The storage mechanism in the diode structure disclosed by Sakata is a product of pure speculation.

The diode structure of Sakata is so fundamentally different from the structure of a traditional transistor that there is no possible suggestion in Sakata for the modification of the Examiner. The words source, drain, and channel do not appear in Sakata. Furthermore, those skilled in the art understand that a conventional transistor has a channel region that induces the transport of only one type of majority charge carrier, a p-type channel for holes or an n-type channel for electrons. In contrast, the diode structure of Sakata receives both electrons and holes. "By applying a negative (positive) gate bias, holes (electrons) are injected from the substrate into the a-Si:H layer through the graded a-SiC:H layer and recombine with the stored electrons (holes) and thus the memory is erased." Sakata, text bridging columns 1 and 2. The diode structure of Sakata and its operation are clearly substantially different from a traditional transistor. The knowledge of ordinary transistors by those skilled in the art would not supply a suggestion to modify the diode of Sakata that is so different in structure and operation.

The Examiner is relying on two statements in Sakata regarding memory devices. Sakata states that "the HJ structure shown in Fig. 1 can be applied to floating-gate memory devices." Sakata, column 1. Later, Sakata states that "the present structure can be used as a component of dynamic random access memories (DRAMS)." Sakata, column 3. These statements are not clear and particular, and are not technically consistent. Sakata may not be familiar with DRAMs

and floating-gate memory devices which are entirely different, and operate differently with different devices. DRAMs have transistors and capacitors to store data, while floating-gate memory devices use floating-gate transistors. On the other hand, Sakata may be merely expressing the hope that the diode structure can be used in some unspecified type of memory device. The C-V plot of Sakata shows a "large hysteresis" that may be used as a memory window. Sakata, column 2. While the hysteresis shown in the C-V plot may be used to create a device to store data, this is **not** a clear and particular suggestion that the diode structure of Sakata is similar to a traditional transistor in any way, or that it has a source region, a drain region, and a channel region.

The applicant respectfully submits that Sakata does not disclose or suggest all of the elements recited in claim 24, and that claim 24 is in condition for allowance. Claims 25-28 and 44 are dependent on claim 24, and recite further limitations with respect to claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 25-28 and 44 are not disclosed or suggested by Sakata, and that claims 25-28 and 44 are in condition for allowance.

Claims 2, 3, 41, 45, 46, 50, and 65 recite elements similar to those recited in claim 24. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 2, 3, 41, 45, 46, 50, and 65 are not disclosed or suggested by Sakata, and that claims 2, 3, 41, 45, 46, 50, and 65 are in condition for allowance.

Claims 31, 35, 38, 40, 42, 43, 47-49, 51-64, 66 and 67 were rejected under 35 USC § 103(a) as being unpatentable over Sakata in view of Sugita et al. (JP Patent No. 08-255878, Sugita). The applicant respectfully traverses.

Claims 31, 35, 38, 40, 49, and 53-64 have been cancelled.

Claims 42, 43, 47, and 51 are dependent on claims 2, 3, 46, and 50, respectively. Claims 2, 3, 46, and 50 were discussed above with respect to the rejection based on Sakata. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 42, 43, 47, and 51 are not disclosed or suggested by the combination of Sakata and Sugita, and that claims 42, 43, 47, and 51 are in condition for allowance.

Claim 48 recites a transistor comprising, among other elements, a floating gate and a polysilicon control gate separated from the floating gate by a layer of insulating material.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143.

The applicant respectfully submits that the Examiner has not met the first and third criteria. With regard to the third criteria, Sakata discloses a diode structure of stacked insulator layers with a metal gate. Sugita discloses a floating gate transistor with a polysilicon floating gate and a control gate, but is silent with respect to the material of the control gate. Neither Sakata nor Sugita disclose or suggest the polysilicon control gate recited in claim 48. Therefore, even as combined, Sakata and Sugita do not disclose or suggest all of the elements recited in claim 48.

With regard to the first criteria, the Examiner stated that it would have been obvious to one skilled in the art in view of Sakata and Sugita to substitute the polysilicon material of the floating gate of Sugita for the metal gate of Sakata. There is no suggestion in either Sakata or Sugita for this combination for many reasons, including the fact that even Sugita does not disclose a polysilicon control gate. The Examiner has stated that Sakata and Sugita are combinable because they are from the same field of endeavor. This is not a suggestion that will satisfy MPEP 2143, or the case law discussed above. The Examiner further stated that the motivation for modifying Sakata is that "polysilicon is a well known conductor in the art as established by Sugita." Final rejection, page 11. This is a fact which does not provide a motivation for changing Sakata. There is no disclosure that Sakata would be improved by this modification. The Examiner is improperly using hindsight to piece together the claimed invention from elements in the prior art without any motivation from the prior art.

The applicant respectfully submits that the Examiner has not established a *prima facie* case of obviousness as is required by MPEP 2143. The applicant respectfully submits that claim

48 is not disclosed or suggested by Sakata and Sugita, and that claim 48 is in condition for allowance. Claim 66 is dependent on claim 48, and recites further limitations with respect to claim 48. For reasons analogous to those stated above, and the limitations in the claim, the applicant respectfully submits that claim 66 is not disclosed or suggested by Sakata and Sugita, and that claim 66 in condition for allowance.

Claims 52 and 67 recite elements similar to those recited in claim 48. For reasons analogous to those stated above, and the limitations in the claims, the applicant respectfully submits that claims 52 and 67 are not disclosed or suggested by Sakata and Sugita, and that claims 52 and 67 are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 5 SEPTEMBER 2001 By _____

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box RCE, Commissioner of Patents, Washington, D.C. 20231, on this 5th day of September, 2001.

Name Amy Moriarty

Signature Amy Moriarty